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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,190	06/30/2003	Bruce B. Doris	FIS920030152	1189

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INTERNATIONAL BUSINESS MACHINES CORPORATION
DEPT. 18G
BLDG. 300-482
2070 ROUTE 52
HOPEWELL JUNCTION, NY 12533

EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 11/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/604,190	DORIS ET AL.	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) *18-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,13-15,17,21 and 22* is/are rejected.

7)☒ Claim(s) *8-12 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 June 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/02/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 02/02/2006 has been entered.

Election/ Restriction

2. Claims 18-20 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 06/15/2004.

Drawings

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: "transition region **R**", paragraph [0035]). The drawings are also objected to because lead line **80**, Fig. 3(b), points to two different parts or points to a different part. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing

on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter that the applicant regards as his invention.

4. **Claim 5** is rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 5 recites "a width transition region" which is not distinct. Specifically, it is not clear which width said width transition region refers to: the first width, the second width, or a width of numerous other elements of the semiconductor device structure. Since there could be a number of different widths, said a width transition region is not distinct, not particular, and therefore indefinite.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. **Claims 1-2, 6-7, and 13-15, 17, and 21** are rejected under 35 U.S.C. 102(e) as being anticipated by Huang et al. U.S. Patent Application Publication 2004/0104405 (the '405 reference, cited in a previous office action).

The '405 reference discloses in Fig. 3 and respective portions of the specification a semiconductor device structure as claimed.

Referring to **claim 1**, the reference discloses a semiconductor device structure, comprising:

at least first and second field effect transistors (NMOS and PMOS, Fig. 3) disposed on a substrate (10);

said first field effect transistor (NMOS) including a first spacer (22) having a first width;

said second field effect transistor (PMOS) including a second spacer (40'; because there is no standard definition for "spacer" and because Applicant has not clearly defined "spacer" so as to put one of ordinary skill in the art on notice that the applicant intended to so define that claim term, "spacer" is broadly interpreted, as in component or device that holds two parts at a distance from each other [1], and as such, layer 40' is a spacer between, for example, gate 30 and layer 50; as another example for the use of the term "spacer", **spacer 170**, Fig. 3(b), spacer 260, Fig. 9, spacer 290, Fig. 13, of the present invention) having a second width;

wherein said second spacer (40') includes a first compressive stress material ("silicon nitride", paragraph [0048]), and please note that layer 40' is formed from layer 40, paragraph [0030]), and said structure further comprises a tensile stress material (generally indicated at 50, paragraph [0034]: "Second stress layer 50 is (1) .... and is a (2) a tensile-stress layer is the patterned first stress layer 40' is comprised of a compression-stress layer") disposed on said at least first and second field effect transistors.

1

spacer

Mechanical Devices:
1. Any component or device that holds two parts at a distance from each other. Also, **spacer block**.
2. A wooden piece that fits between charges to lengthen an explosive column.
Engineering:
1. In
spacer. Academic Press Dictionary of Science and Technology (1992). Retrieved 08 November 2006, from xreferplus. http://www.xreferplus.com/entry/3160882

Referring to **claim(s) 2**, the reference further discloses that said first field effect transistor (NMOS) is an nFET ("NMOS") and said second field effect transistor (PMOS) is a pFET ("PMOS").

Referring to **claim(s) 6**, Fig. 3 clearly depicts that said first spacer (22) includes an I-shaped part and said second spacer (40') includes an L-shaped part.

Referring to **claim(s) 7**, the reference further discloses that said second spacer includes an L-shaped part and said first compressive stress material, as detailed above for claims 1 and 6.

Referring to **claim(s) 13-14**, the reference further discloses that said first compressive stress material (40') is a dielectric ("silicon nitride") and is silicon nitride (as detailed above for claim 1).

Referring to **claim(s) 15**, the reference further discloses that said tensile stress material (generally indicated at 50) is SiN ("silicon nitride", paragraph [0043]).

Referring to **claim(s) 17**, the reference further discloses that said tensile stress material (50) is a layer (50) having a substantially uniform thickness in a range of about 20 nm to about 70nm ("200 to 700 Å", paragraph [0034]), overlapping the claimed range of about 20 nm to about 100 nm.

Referring to **claim(s) 21**, the reference further discloses that said substrate (10) is a silicon substrate (paragraph [0025]).

6. Claims 1-3, 6-7, and 13-15, 17, and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Hachimine et al. U.S. Patent Application Publication 2003/0181005 (the '005 reference).

The '405 reference discloses in Fig. 24; a modified form of embodiment 1 of Fig. 1, and respective portions of the specification a semiconductor device structure as claimed.

Referring to **claim 1**, the reference discloses a semiconductor device structure, comprising:

at least first and second field effect transistors (n-ch MISFET 1n and p-ch MISFET 1p, Fig. 24) disposed on a substrate (generally indicated at 1/2/3);

said first field effect transistor (1n) including a first spacer (9) having a first width (about 50-70 nm, paragraph [0187]);

said second field effect transistor (1p) including a second spacer (14b; "spacer" is broadly interpreted) having a second width (about 100 nm, paragraph [0202]);

wherein said second spacer (14b) includes a first compressive stress material ("silicon nitride", paragraph [0168]), and said structure further comprises a tensile stress material (generally indicated at 14a, "silicon nitride", paragraph [0168]) disposed on said at least first and second field effect transistors.

Referring to **claim(s) 2**, the reference further discloses that said first field effect transistor (1n) is an nFET ("n-ch MISFET") and said second field effect transistor (1p) is a pFET ("p-ch MISFET").

Referring to **claim(s) 3**, the reference further discloses that said first width (50-70 nm, as detailed above) is less than said second width (about 100 nm, as detailed above).

Referring to **claim(s) 6**, Fig. 24 clearly depicts that said first spacer (9) includes an I-shaped part and said second spacer (14b) includes an L-shaped part.

Referring to **claim(s) 7**, the reference further discloses that said second spacer includes an L-shaped part and said first compressive stress material, as detailed above for claims 1 and 6.

Referring to **claim(s) 13-14**, the reference further discloses that said first compressive stress material ("silicon nitride") is a dielectric and is silicon nitride (as detailed above for claim 1).

Referring to **claim(s) 15**, the reference further discloses that said tensile stress material is SiN ("silicon nitride", as detailed above for claim 1).

Referring to **claim(s) 17**, the reference further discloses that said tensile stress material ("silicon nitride") is a layer (14a) having a substantially uniform thickness in a range of about 100 - 120 nm (paragraph [0194]), overlapping the claimed range of about 20 nm to about 100 nm.

Referring to **claim(s) 21**, the reference further discloses that said substrate (1/2/3) is a silicon substrate (paragraph [0164]).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. **Claim 4** is rejected under 35 U.S.C. §103(a) as being unpatentable over Huang et al. U.S. Patent Application Publication 2004/0104405 (the '405 reference, cited in a previous office action).

Referring to **claim 4**, the '405 reference discloses a semiconductor device structure substantially as claimed and as detailed above for claim 1, including said nFET and said pFET. However, the reference does not disclose that said structure is an inverter as claimed. Nevertheless, because the reference also does not particularly exclude such usage, such a utilization of said nFET and said pFET to form an inverter would have been obvious to one of ordinary skill in the art at the time the invention was made.

8. **Claim 22** is rejected under 35 U.S.C. §103(a) as being unpatentable over Huang et al. U.S. Patent Application Publication 2004/0104405 (the '405 reference, cited in a previous office action) in view of Huotari U.S. Patent Application Publication 2004/0106249.

The '405 reference discloses a semiconductor device structure as claimed and as detailed above for claims 1 and 21, including said NMOS transistor and said PMOS transistor on said silicon substrate. However, the reference does not teach that said substrate could comprise GaAs. In other words, the reference does not disclose that said substrate is a GaAs substrate.

Nevertheless, Huotari, in disclosing a semiconductor device structure including an NMOS transistor and a PMOS transistor on a substrate, teaches that the substrate could be a silicon substrate or a GaAs substrate (paragraph [0035]), thereby teachings that the two materials for the substrate are art equivalents.

9. **Claim 4** is rejected under 35 U.S.C. §103(a) as being unpatentable over Hachimine et al. U.S. Patent Application Publication 2003/0181005 (the '005 reference).

Referring to **claim 4**, the '005 reference discloses a semiconductor device structure substantially as claimed and as detailed above for claim 1, including said nFET and said pFET. However, the reference does not disclose that said structure is an inverter as claimed. Nevertheless, because the reference also does not particularly exclude such usage, such a utilization of said nFET and said pFET to form an inverter would have been obvious to one of ordinary skill in the art at the time the invention was made.

10. **Claim 22** is rejected under 35 U.S.C. §103(a) as being unpatentable over Hachimine et al. U.S. Patent Application Publication 2003/0181005 (the '005 reference) in view of Huotari U.S. Patent Application Publication 2004/0106249.

The '405 reference discloses a semiconductor device structure as claimed and as detailed above for claims 1 and 21, including said nFET and said pFET on said silicon substrate. However, the reference does not teach that said substrate could comprise GaAs. In other words, the reference does not disclose that said substrate is a GaAs substrate.

Nevertheless, Huotari, in disclosing a semiconductor device structure including an nFET (NMOS transistor) and a pFET (PMOS transistor) on a substrate, teaches that the substrate could be a silicon substrate or a GaAs substrate (paragraph [0035]), thereby teachings that the two materials for the substrate are art equivalents.

Allowable Subject Matter

11. Claim 8-12 and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for the indication of allowable subject matter: The cited art, whether taken singularly or in combination, especially when all limitations are considered within the claimed specific combination, fails to teach or render obvious a semiconductor device structure having all exclusive limitations as recited in claims 8, 9, 10, 11, 12, and 16.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 7:30 am - 6:00 pm, Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Minsun Harvey can be reached on (571) 272-1835. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tu-Tu Ho
November 09, 2006